CLAIMS

What is claimed is:

1. A method comprising:

selectively depositing a collar material between a number of memory containers, wherein the collar material along a side of a first memory container of the number of memory containers is in contact with the collar material along a side of a second memory container, and wherein an opening exists between the collar material along a corner of the first memory container and the collar material along a corner of a third memory container.

2. The method of claim 1, wherein selectively depositing the collar material between the number of memory containers comprises selectively depositing a boron-doped carbon film material between the number of memory containers.

3. The method of claim 1, wherein at least one side of the number of memory containers includes a double-sided capacitor.

4. The method of claim 3, wherein an electrode of the double-sided capacitor includes poly silicon.

5. The method of claim 1, wherein selectively depositing the collar material between the number of memory containers comprises selectively depositing the collar material on a borophosphosilicate glass between the number of memory containers.

6. The method of claim 1, wherein selectively depositing the collar material between the number of memory containers comprises selectively depositing the collar material on a tetraethylortho-silicate material between the number of memory containers.

7. A method for forming an array of memory, the method comprising:

forming a number of memory containers in a mold, wherein a first memory container of the number of memory containers is located in a first direction from a first adjacent memory container of the number of memory containers and wherein the first memory container is located in a second direction from a second adjacent memory container of the number of memory containers; and

depositing a collar material between the number of memory containers, wherein a part of the collar material along a side wall of the first memory container is in contact with a part of the collar material along a side wall of the first adjacent container in the first direction and wherein a part of the collar material along a second side wall of the first memory container is not in contact with a part of the collar material along a side wall of the second adjacent container in the second direction.

8. The method of claim 7, wherein forming the number of memory containers in the mold comprises forming the first memory container to be substantially diagonal to the second adjacent memory container.

9. The method of claim 7, wherein forming the number of memory containers in the mold comprises forming the number of memory containers in a borophosphosilicate glass.

10. The method of claim 7, wherein forming the number of memory containers in the mold comprises forming the number of memory containers in a tetraethylortho-silicate.

11. The method of claim 7, wherein forming the number of memory containers in the mold comprises forming the number of memory containers in SiLK.

12. A method comprising:

arranging a number of memory containers in a mold, wherein a first memory container of the number of memory containers is located in a first direction from a first adjacent memory container of the number of memory containers and wherein the first memory container is located in a second direction from a second adjacent memory container of the number of memory containers; and

depositing a collar material between the number of memory containers, wherein a part of the collar material along a side of the first memory container is in contact with a part of the collar material along a side of the first adjacent container in the first direction and wherein a part of the collar material along a second side of the first memory container is not in contact with a part of the collar material along a side of the second adjacent container in the second direction.

13. The method of claim 12, further comprising removing the mold through an opening between the second side of the first memory container and the side of the second adjacent container.

14. The method of claim 13, wherein removing the mold through the opening between the second side of the first memory container and the side of the second adjacent container comprises etching the mold through the opening with hydrogen fluoride.

15. The method of claim 12, further comprising removing the collar material.

16. The method of claim 12, wherein arranging the number of memory containers in the mold comprises arranging the number of memory containers in phosphosilicate glass.

17. The method of claim 12, wherein arranging the number of memory containers in the mold comprises arranging the number of memory containers in a tetraethylortho-silicate.

18. A method of fabricating an integrated circuit, the method comprising:

arranging a number of semiconductor containers in a borophosphosilicate glass (BPSG) material, wherein a first semiconductor container of the number of semiconductor containers is located a first distance, S, from a first adjacent semiconductor container of the number of memory semiconductor in a first direction and wherein the first semiconductor container is located a second distance, L, from a second adjacent semiconductor container of the number of semiconductor containers in a second direction;

selectively depositing a collar material as spacers along side walls of the semiconductor containers, wherein the spacers are thicker than S/2 and thinner than L/2;

performing a dry etch to remove the BPSG material between the first semiconductor container and the second adjacent semiconductor container along the second direction; and

performing a selective wet etch to remove remaining BPSG material.

19. The method of claim 18, wherein selectively depositing a collar material comprises selectively depositing a boron-doped carbon film material.

20. The method of claim 18, wherein selectively depositing a collar material comprises selectively depositing a silicon nitride material.

21. The method of claim 18, further comprising removing the collar material after performing the dry etch and performing the selective wet etch.

22. The method of claim 21, wherein removing the collar material comprises plasma etching the collar material.

23. The method of claim 22, wherein plasma etching the collar material comprises plasma etching the collar material at a pressure at approximately 1 Torr.

24. A method comprising:

forming a number of memory containers in a mold, wherein a first memory container of the number of memory containers is located a first distance, S, from a first adjacent memory container of the number of memory containers in a first direction and wherein the first memory container is located a second distance, L, from a second adjacent memory container of the number of memory containers in a second direction;

etching the mold to a depth that is at least greater than the second distance, L;

depositing a collar material between the number of memory containers;

selectively removing the collar material, wherein the collar material is thicker than S/2 and thinner than L/2 along side walls of the number of memory containers;

removing the mold located between the first memory container and the second adjacent memory container between the collar material;

removing remaining mold; and

removing the collar material.

25. The method of claim 24, wherein forming the number of memory containers in a mold comprises forming the number of memory containers in phosphosilicate glass.

26. The method of claim 24, wherein forming the number of memory containers in the mold comprises forming the number of memory containers in tetraethylortho-silicate.

27. The method of claim 24, wherein forming the number of memory containers in the mold comprises forming the number of memory containers in SiLK.

28. The method of claim 24, wherein depositing the collar material between the number of memory containers comprises depositing silicon nitride between the number of memory containers.

29. The method of claim 24, wherein removing the mold located between the first memory container and the second adjacent memory container between the collar material comprises performing a dry etch of the mold located between the first memory container and the second adjacent memory container between the collar material.

30. The method of claim 24, wherein removing the mold located between the first memory container and the second adjacent memory container between the collar material comprises etching of the mold, using an acetic acid and hydrogen fluoride, located between the first memory container and the second adjacent memory container between the collar material.

31. A method for fabricating an array of memory cells, the method comprising:

forming a number of memory containers in a borophosphosilicate glass (BPSG) material, wherein a first memory container of the number of memory containers is located in a first direction from a first adjacent memory container of the number of memory containers and wherein the first memory container is located in a second direction from a second adjacent memory container of the number of memory containers;

depositing a collar material, comprised of silicon nitride, between the number of memory containers, wherein the collar material along a side wall of the first memory container is in contact with the collar material along a side wall of the first adjacent container in the first direction and wherein the collar material along a second side wall of the first memory container is not in contact with the collar material along a side wall of the second adjacent container in the second direction;

performing a dry etch to remove the BPSG material located between the first memory container and the second adjacent memory container between the collar material; and

performing a wet etch to remove remaining BPSG material.

32. The method of claim 31, wherein performing the wet etch to remove remaining BPSG material comprises performing a hydrogen fluoride-based wet etch to remove remaining BPSG material.

33. The method of claim 31, wherein forming the number of memory containers in the BPSG material comprises forming a liner comprised of titanium nitride within the number of memory containers.

34. The method of claim 31, wherein forming the number of memory containers in the BPSG material comprises forming an electrode comprised of poly silicon.

35. The method of claim 31, further comprising etching the collar material based on an H_2 plasma.

36. A method for forming a memory array, the method comprising:

forming a number of memory containers in a tetraethylortho-silicate (TEOS), wherein a first memory container of the number of memory containers is located in a first direction from a first adjacent memory container of the number of memory containers and wherein the first memory container is located in a second

direction from a second adjacent memory container of the number of memory containers; and

depositing a collar material, that includes boron doped carbon film, between the number of memory containers, wherein the collar material along a first side wall of the first memory container is in contact with the collar material along a side wall of the first memory adjacent container in the first direction and wherein the collar material approximately along a corner of the first memory container is not in contact with the collar material approximately along a corner of the second adjacent memory container in the second direction.

37. The method of claim 36, further comprising dry etching, with hydrogen fluoride, the TEOS located between the corner of the first memory container and the corner of the second adjacent memory container in the second direction.

38. The method of claim 37, further comprising wet etching remaining TEOS.

39. The method of claim 38, further comprising etching the collar material with H_2-based plasma.

40. The method of claim 39, wherein etching the collar material with H_2-based plasma includes etching the collar material with H_2-based plasma at a pressure of approximately 1 Torr.

41. The method of claim 36, further comprising depositing a spin-on glass on the number of memory containers prior to depositing the collar material.

42. A method for forming an integrated circuit, the method comprising:

forming a number of memory containers in a mold on a substrate, wherein a first memory container of the number of memory containers is located in a first direction from a first adjacent memory container of the number of memory

containers and wherein the first memory container is located in a second direction from a second adjacent memory container of the number of memory containers;

depositing a negative tone resist over the substrate; and

forming a pattern in the negative tone resist, wherein an opening is formed between the first memory container and the second adjacent memory container.

43. The method of claim 42, wherein forming the number of memory containers in a mold on the substrate comprises forming the number of memory containers in a phosphosilicate glass on the substrate.

44. The method of claim 42, wherein forming the number of memory containers in a mold on the substrate comprises forming the number of memory containers in a tetraethylortho-silicate on the substrate.

45. The method of claim 42, wherein forming the number of memory containers in a mold on the substrate comprises forming the number of memory containers in a SiLK on the substrate.

46. A method for forming a memory, the method comprising:

forming a number of memory containers in a mold on a substrate, wherein a first memory container of the number of memory containers is located in a first direction from a first adjacent memory container of the number of memory containers and wherein the first memory container is located in a second direction from a second adjacent memory container of the number of memory containers;

depositing a positive tone resist over the substrate; and

vapor etching the mold, through the positive tone resist, between the number of memory containers on the substrate.

47. The method of claim 46, wherein the vapor etching of the mold comprises vapor etching the mold with hydrogen fluoride.

48. The method of claim 46, wherein forming the number of memory containers in a mold on the substrate comprises forming the number of memory containers in a borophosphosilicate glass on the substrate.

49. The method of claim 46, wherein forming the number of memory containers in a mold on the substrate comprises forming the number of memory containers in a tetraethylortho-silicate on the substrate.

50. An array of memory cells comprising:

a substrate;

a number of memory containers formed on the substrate, wherein a first memory container of the number of memory containers is located a first distance, S, from a first adjacent memory container of the number of memory containers in a first direction and wherein the first memory container is located a second distance, L, from a second adjacent memory container of the number of memory containers in a second direction, wherein S is less than L; and

a collar comprised of silicon nitride and formed on external side walls of the number of memory containers, wherein the collar formed on the external side walls is thicker than S/2 and thinner than L/2.

51. The array of memory cells of claim 50, wherein the number of memory containers are formed on the substrate by:

dry etching mold located between the first memory container and the second adjacent memory container between the collar material; and

wet etching mold under the collar.

52. The array of memory cells of claim 51, wherein the mold includes borophosphosilicate glass.

53. The array of memory cells of claim 51, wherein the mold includes tetraethylortho-silicate.

54. The array of memory cells of claim 51, wherein the mold includes SiLK.

55. The array of memory cells of claim 50, wherein the number of memory containers have at least one side wall that includes a double-sided capacitor.

56. An integrated circuit device comprising:

a substrate; and

an array of memory cells formed, using a number of memory containers, on the substrate by:

selectively depositing a collar material between the number of memory containers, wherein a part of the collar material along a side wall of a first memory container of the number of memory containers is in contact with a part of the collar material along a side wall of a second memory container, and wherein an opening exists between a part of the collar material along a corner of the first memory container and a part of the collar material along a corner of a third memory container.

57. The integrated circuit device of claim 56, wherein the collar material includes a boron-doped carbon film.

58. The integrated circuit device of claim 56, wherein at least one side of the number of memory containers includes a double-sided capacitor.

59. The integrated circuit device of claim 58, wherein an electrode of the double-sided capacitor includes poly silicon.

60. A memory device comprising:

a substrate; and

a number of memory cells fabricated on the substrate by:

forming a number of memory containers in a mold, wherein a first memory container of the number of memory containers is located a first distance, S, from a first adjacent memory container of the number of memory containers in a first direction and wherein the first memory container is located a second distance, L, from a second adjacent memory container of the number of memory containers in a second direction;

etching the mold to a depth that is at least greater than the second distance, L;

depositing a collar material between the number of memory containers;

selectively removing the collar material, wherein the collar material is thicker than S/2 and thinner than L/2 along side walls of the number of memory containers;

dry etching the mold located between the first memory container and the second adjacent memory container between the collar material;

wet etching the remaining mold on the substrate; and

etching the collar material.

61. The memory device of claim 60, wherein the mold includes phosphosilicate glass.

62. The memory device of claim 60, wherein the mold includes tetraethylortho-silicate.

63. The memory device of claim 60, wherein the mold includes SiLK.

64. The memory device of claim 60, wherein the collar material includes silicon nitride.

65. A memory comprising:

an array of memory cells formed by:

fabricating a number of memory containers in a tetraethylortho-silicate (TEOS), wherein a first memory container of the number of memory containers is located in a first direction from a first adjacent memory container of the number of memory containers and wherein the first memory container is located in a second direction from a second adjacent memory container of the number of memory containers; and

depositing a collar material, that includes boron doped carbon film, between the number of memory containers, wherein the collar material along a first side wall of the first memory container is in contact with the collar material along a side wall of the first memory adjacent container in the first direction and wherein the collar material approximately along a corner of the first memory container is not in contact with the collar material approximately along a corner of the second adjacent memory container in the second direction.

66. The memory of claim 65, wherein the array of memory cells is further formed by dry etching, with hydrogen fluoride, the TEOS located between the corner of the first memory container and the corner of the second adjacent memory container in the second direction.

67. The memory of claim 65, wherein the array of memory cells is further formed by wet etching remaining TEOS.

68. The memory of claim 65, wherein the array of memory cells is further formed by etching the collar material with H_2-based plasma.

69. An apparatus comprising:

an address decoder to decode at least one memory access request; and

a memory coupled to the address decoder, wherein data stored in a number of memory cells in the memory is accessed based on the at least one decoded memory access request, wherein the number of memory cells are formed by:

forming a number of memory containers in a mold on a substrate, wherein a first memory container of the number of memory containers is located in a first direction from a first adjacent memory container of the number of memory containers and wherein the first memory container is located in a second direction from a second adjacent memory container of the number of memory containers;

depositing a negative tone resist over the substrate; and

forming a pattern in the negative tone resist, wherein an opening is formed between the first memory container and the second adjacent memory container.

70. The apparatus of claim 69, wherein the mold includes phosphosilicate glass.

71. The apparatus of claim 69, wherein the mold includes tetraethylortho-silicate

72. The apparatus of claim 69, wherein the mold includes SiLK.

73. The apparatus of claim 69, wherein at least one side of the number of memory containers includes a double-sided capacitor.

74. The apparatus of claim 73, wherein an electrode of the double-sided capacitor is comprised of poly silicon.

75. The apparatus of claim 73, wherein an electrode of the double-sided capacitor is comprised of titanium nitride.

76. A system comprising:

a processor; and

a memory circuit coupled to the processor, wherein the memory circuit includes a semiconductor device comprising:

a number of memory containers formed over a semiconductor structure; and

a collar comprised of an insulator material and formed on side walls of the number of memory containers, wherein the collar connects together a first memory container to a second memory container of the number of memory containers along a first direction and wherein the collar does not connect together the first memory container to a third memory container along a second direction.

77. The system of claim 76, wherein the insulator material includes silicon nitride.

78. The system of claim 76, wherein the insulator material includes a boron-doped carbon film material.

79. An electronic system comprising:

a processor to execute a number of instructions; and

a memory to store at least a part of the number of instructions, the memory having a number of memory cells, wherein the number of memory cells includes a double-sided capacitor fabricated in side walls of a number of memory containers, the number of memory cells fabricated by:

forming the number of memory containers in a mold, wherein a first memory container of the number of memory containers is located in a first direction from a first adjacent memory container of the number of memory containers and wherein the first memory container is located in a second direction from a second adjacent memory container of the number of memory containers; and

depositing a collar material between the number of memory containers, wherein a part of the collar material along a side wall of the first memory container is in contact with a part of the collar material along a side wall of the first adjacent container in the first direction and wherein a part of the collar material along a second side wall of the first memory container is not in contact with a part of the collar material along a side wall of the second adjacent container in the second direction.

80. The electronic system of claim 79, wherein the first memory container is substantially diagonal to the second adjacent memory container.

81. The electronic system of claim 79, wherein the mold includes a borophosphosilicate glass.

82. The electronic system of claim 79, wherein the mold includes a tetraethylortho-silicate.

83. The electronic system of claim 79, wherein the mold includes SiLK.

84. The electronic system of claim 79, wherein the collar material includes silicon nitride.

85. The electronic system of claim 79, wherein the collar material includes a boron-doped carbon film material.

86. A system comprising:

a processor;

a memory device coupled to the processor for storage of instructions that the processor is to execute, the memory device comprising:

an array of memory cells formed by:

selectively depositing a silicon nitride collar between a number of memory containers, wherein the silicon nitride collar along a side of a first memory container of the number of memory containers is in contact with the silicon nitride collar along a side of a second memory container, and wherein an opening exists between the silicon nitride collar along a corner of the first memory container and the silicon nitride collar along a corner of a third memory container.

87. The system of claim 86, wherein at least one side of the number of memory containers includes a double-sided capacitor.

88. The system of claim 87, wherein an electrode of the double-sided capacitor includes poly silicon.

89. The system of claim 87, wherein an electrode of the double-sided capacitor includes titanium nitride.

90. The system of claim 86, wherein selectively depositing the silicon nitride collar between the number of memory containers comprises selectively depositing the silicon nitride collar on a borophosphosilicate glass between the number of memory containers.

91. The system of claim 86, wherein selectively depositing the collar material between the number of memory containers comprises selectively depositing the collar material on a tetraethylortho-silicate material between the number of memory containers.